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Modelling and Simulation of Single Phase Multilevel Inverter with Minimum Power Devices and DC Sources

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Abstract:*The Multilevel inverter (MLI) are the preferred choice in industry for the application of medium and high power application. Though multilevel inverter has a number of favour and also has disadvantages in the way of achieving the higher [levels] because of using more amount of semiconductor devices. This may lean towards to increase the installation cost and area. Hence to overthrown this problem the new multilevel inverter is introduced with minimum number of power electronic components. The proposed method is appropriate for high power application with minimum quantity of devices. Phase disposition PWM technique is used for switching signal generation. The results are validated using MATLAB/Simulink and it is implemented in SPARTAN6 FPGA Kit.*

Keywords*: Multilevel Inverter (MLI), Phase Disposition Pulse Width Modulation, Field Programmable Gate Array (FPGA);*

I. Introduction

Now a days, multilevel inverters has drawn large interest from the diligence exhausting medium-voltage and high power solicitations. Multilevel inverters generate many voltage levels. A preferred output voltage waveform can be symphonized from the multiple voltage levels with low bias, low switching frequency, higher competence, and lower voltage devices.Yet, it requires a huge quantity of circuit modules[1]-[5].In conservative multilevel inverters, a cascaded H-bridge multilevel inverter (CHB) is the solitary preferred choice to upsurge the amount of output voltage levels. However, the H-bridge cells by increasing the CHB, and it also increases power electronic devices [6]-[7]. The superlative elucidations to generate the highest yield of voltage stages by minimize the quantity of circuit apparatuses in a CHB is to use asymmetrical dc voltage[8]-[9]. The H converters which are coupled to the each phase inverter which is connected to the same DC link by scaling the source with the power of three. Conversely for up surging the voltage level, which increases the dc voltage source. The cascaded transformer is employed [10] with six floating power supplies are used to alleviate this problem. Due to the usage of cascaded transformer the system becomes hulky. To elude this difficulty, the proposed multilevel inverter engaging four floating power supplies are included[11].Yet to obtain independent dc voltage source, it also requires front end transformer so transformer less circuit topologies are introduced [12]-[18].In [12], a packed U-cell multilevel inverter topology stood introduced which has reduced amount of circuit components. Furthermore it also requires a bulky capacitor of 5000μF which hosts the high ripples. Multilevel inverters retaining bidirectional switches with series-linked capacitors was announced in [13]-[14]. Hypothetically, by reducing the number of circuit components, they can achieve a huge amount of output voltage levels up 125 levels. To generate this a modular multilevel converter was proposed in [15]. It has a good modular characteristic; thus, it is flexible to extend to increasing the voltage stages. Nevertheless, by compared with other rival it

surges the amount of hulking capacitors and switches. A multilevel inverter using series-connected dc voltage sources was recommended in [16]. It includes two stages one of them is a level-spawning stage and second stage is polarity generating part to lessen the switching losses. Yet, it flops to curtail the amount of dc voltage sources by increasing the output voltage stages. A multilevel inverter engaging switched series/parallel dc voltage sources was introduced in [17]. Despite it can growth the amount of output voltage stages, but the switching pattern is multifaceted, and it transmission fatalities will be high. A photovoltaic multilevel inverter using series-linked capacitors was labouring in [18]. It do not clarify about the capacitor voltage balancing. The preceding tactics agreed in [12]–[18] uses series-attached capacitors. This is beneficial to increase the output voltage stages and solves the capacitor voltage destabilizing problematic by minimising the number of independent dc voltage sources. In this manuscript, we introduce a compelling circuit arrangement of a multilevel inverter with a minimised amount of circuit apparatuses. It subsist of a single dc voltage source paralleled to series linked capacitors, two diodes, three switches for incorporating the output voltage levels, and an H-bridge cell. Here, we also propose a modified pulse width modulation (PWM) control strategy to solve the capacitor voltage

destabilizing problem that arose in series connected capacitors. Then the validated output is counterfeit in MATLAB/Simulink and implemented in FPGA kit.

II. Seven Level Pwm Inverter

2.1 Circuit Configuration

Fig. 1shows a circuit arrangement of the 7- level PWM inverter. The 7-level PWM inverter take on single dc voltage source, which is branched by three series linked capacitors. Each capacitor voltage is equivalently branched to *V*dc/3. Then, we can attain the 7- stages in the output voltage wave, i.e., *V*dc, 2*V*dc/3,*V*dc/3, 0, −*V*dc/3, −2*V*dc/3, and −*V*dc. The H-bridge cell includes switches (*S*1∼*S*4) is used to regulate the polarity of the output voltage with the highest (or lowest) voltage level, i.e., *V*dc (or −*V*dc) and remaining voltage levels are generated by *S*5, *S*6, and *S*7.

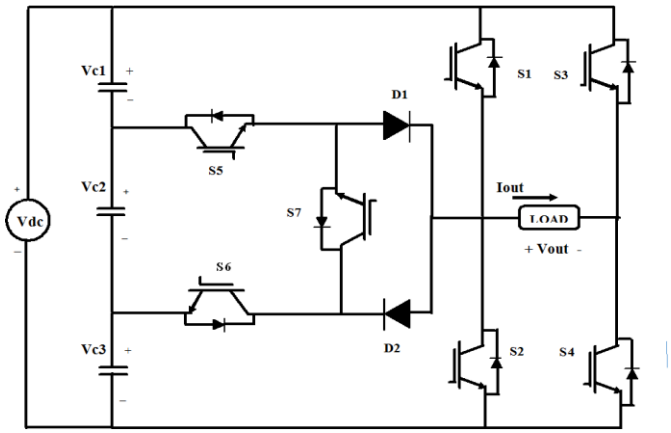


Fig. 1. Circuit arrangement of the seven-level PWM inverter.

2.1.1 Generation of Output Voltage Levels

Level V_{dc}*:* Three series connected capacitors deliveries energy to the output load. It discharges through the switchesS_1 and S_4. If an inductive load is used and the load current is streams in opposite direction, then the current streams overD_{S1} andD_{S4}, and it energies the capacitor mound.

Level 2V_{dc}/3*:* Two capacitors voltage C_2 and C_3 supplies energy to the output load. It discharges over S_5, D_1, and S_4. Here no current flows over during this switching state,when the direction of the load current is opposite. At this moment, the load current streams over D_{S1} and D_{S4}, and it energies the capacitor mound.

Level V_{dc}/3*:* The bottom end capacitor (C_3) supplies energyto the output load. It releases over D_{S6}, S_7, D_1, and S_4. If the direction of the load current is reverse, the load current streams over D_2, S_7, D_{S5}, and D_{S4}.

Level 0: To make a zero level, two switching arrangements can be recognized. The voltage elimination is the elementary notion for generate a zero level. When *S*2 and *S*4 turn on concurrently, the output voltage becomes zero. The alternate scheme is to turn *S*1 and *S*3 on at the same time.

Level −*V*dc/3*:* To generate a *–Vdc/3* voltage level,the upper end capacitor (*C*1) carries energy to the output load.

Level −2*V*dc/3*:* Two capacitors *C*1 and *C*2 carry charges to the output load. When the load current is opposite, it flows through *DS*2 and *DS*3.

Level −*V*dc*:* Three series connected capacitors carries energy to the output load. If the direction of load current is reverse,the current streams over *DS*2 and *DS*3, and it charges the capacitor mound.

2.1.2 General Switching Scheme

Fig. 2shows switching pattern of general phase disposition technique for achieving the 7-level PWM inverter. It contains a reference and three carrier waves. The 3-carrier waves which have the same frequency and but dissimilar amplitudes [19], [20]. By paralleling the reference and each carrier wave, it generates the command signals (C_a, C_b, and C_c). One cycle of the reference voltage is divided into six modes according to the output voltage levels, and the corresponding period(P_n) foreach mode is obtained by

Mode 1 :$P_1 = 0 < \omega t < \theta_1$ and $P_5 = \theta_4 < \omega t < \pi$ (1)

Mode 2 :$P_2 = \theta_1 < \omega t < \theta_2$ and $P_4 = \theta_3 < \omega t < \theta_4$ (2)

Mode 3 :$P_3 = \theta_2 < \omega t < \theta_3$ (3)

Mode 4 :$P_6 = \pi < \omega t < \theta_5$ and $P_{10} = \theta_8 < \omega t < 2\pi$ (4)

Mode 5 :$P_7 = \theta_5 < \omega t < \theta_6$ and $P_9 = \theta_7 < \omega t < \theta_8$ (5)

Mode 6 :$P_8 = \theta_6 < \omega t < \theta_7$. (6)

The switching signals (S_n) are generated by the logical combination of C_a, C_b, C_c, and P_n. By setting the modulation index larger than 0.66 then determine the switching anglesθ_n to generate period (P_n) of each mode for seven level. By using logical expressions AND,OR, and NOT, each switching signal is generated by

$S_1 = \overline{C_a} \cdot (P_6 + P_{10}) + \overline{C_c} \cdot P_3$ (7)

$S_2 = \overline{C_a} \cdot (P_1 + P_5) + \overline{C_c} \cdot P_8$ (8)

$S_3 = P_6 + P_7 + P_8 + P_9 + P_{10}$ (9)

$S_4 = P_1 + P_2 + P_3 + P_4 + P_5$ (10)

$S_5 = C_b \cdot (P_2 + P_4) + C_c \cdot P_3$ (11)

$S_6 = C_b \cdot (P_7 + P_9) + C_c \cdot P_8$ (12)

$S_7 = \overline{C_a} \cdot (P_1 + P_5 + P_6 + P_{10}) + C_b \cdot (P_2 + P_4 + P_7 + P_9)$. (13)

Table I shows switching angle $\theta_n$affording to modulation ratio M_a. For generating the seven level a reference wave and 3- carrier waves are used. Therefore, modulation ratio M_a is calculated by

$$M_a = \frac{A_m}{3A_c} \quad (14)$$

whereA_c is the amplitude of a carrier wave, and A_m is the amplitude of a reference wave. Thus, the output voltage is calculated by

$v_{out} = M_a \sin \omega t$.(15)

When M_a is lessened than 0.33, three levels are generated. When Ma is within the interval of 0.33 and 0.66, the output voltage level has five levels, and with an M_a greater than 0.66, it displays seven output voltage stages.

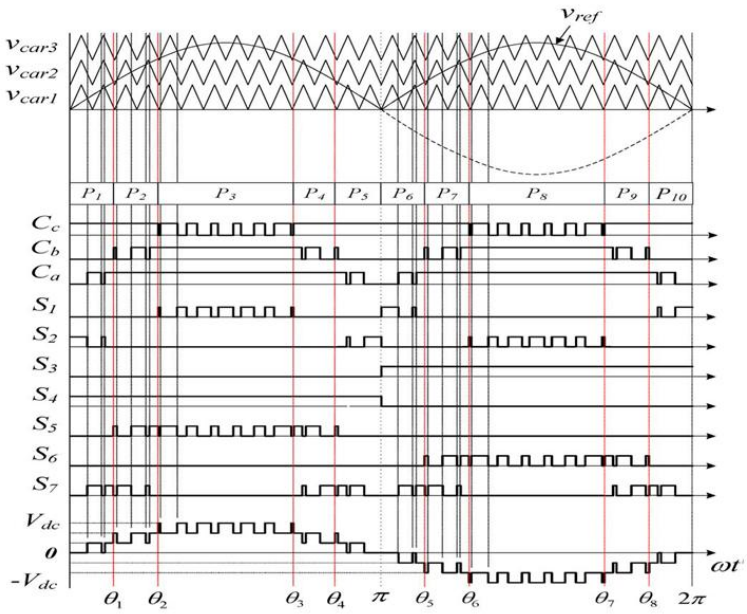


Fig. 2. Switching pattern for generating the seven-level PWM output voltage.

TABLE I Switching Angles According To The Modulation Index

Ma / **Θn**	**Ma < 0.33**	**0.33 < Ma < 0.66**	**Ma > 0.66**
θ1	π/2	Sin^{-1}(Ac/Am)	Sin^{-1}(Ac/Am)
θ2	π/2	π/2	Sin^{-1}(2Ac/Am)
θ3	π/2	π/2	π - θ2
θ4	π/2	π -θ1	π – θ1
θ5	3π/2	π + θ1	π +θ1
θ6	3π/2	3π/2	π +θ2
θ7	3π/2	3π/2	2π–θ2
θ8	3π/2	2π -θ1	2π –θ1

III. FPGA Implementation

The Xilinx ISE design suite 14.3 software used to design the circuit. This software tool for HDL design made by Xilinx intended for synthesis and analysis, then implementing the designer to compile their designs, carry out timing analysis, explore the RTL diagrams, simulate a design's reaction to different stimuli, and design the target device with the programmer.The VHDL code for seven level PWM has been written into the Xilinx ISE design suite. The simulation was validated in the MODELSIM 6.4 a ISE simulator. For generating the sine wave using VHDL program ,the values are taken from the Matlab/simulink.

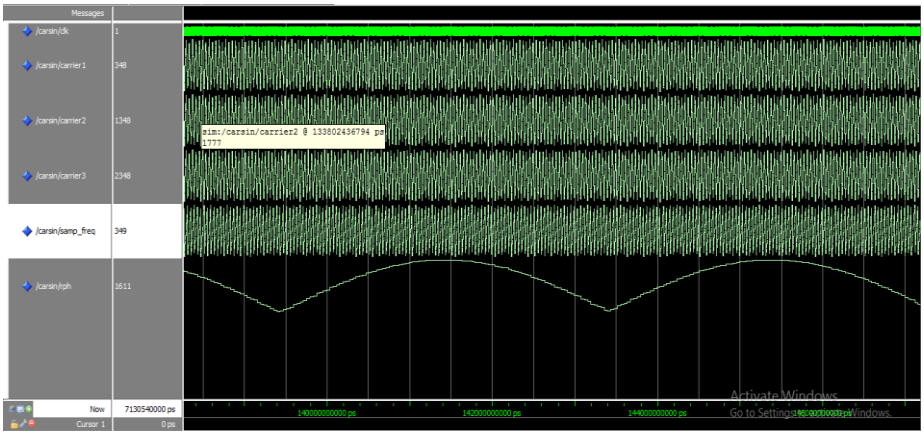


Fig 3.Generation of carrier and reference signal

Then comparing the three carriers and sine wave command signalsC_a,C_b,$C_c$are generated.

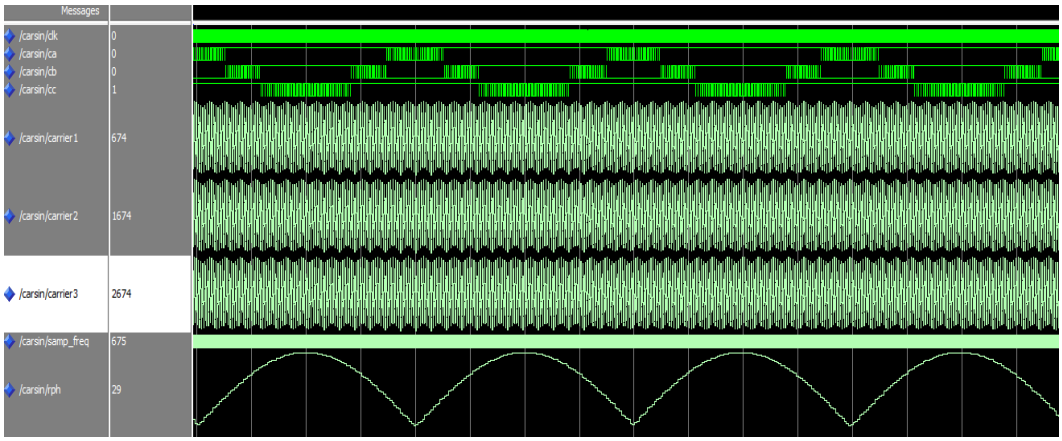


Fig 4. Generation of command signal

By using the generated command signal switching signals are simulated. The period(P_n) is generated according to the switching angle. By using the logical combination of command signals and period (P_n) seven switching signals are generated. Figure.5.shows the generation of switching signal using vhdl coding.

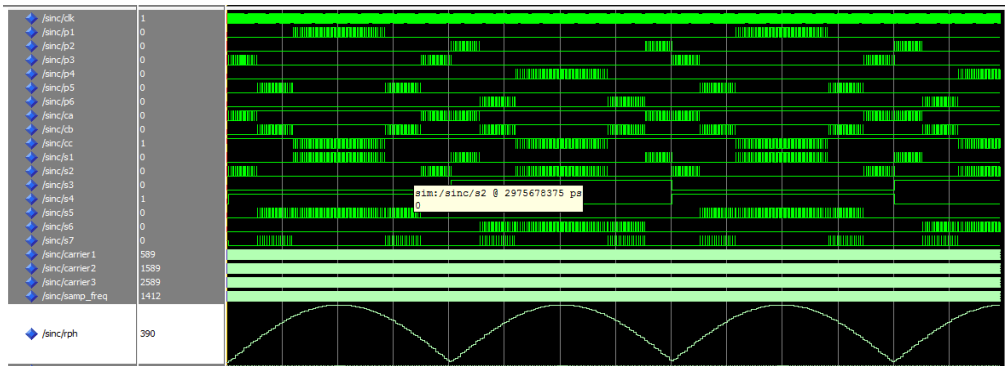


Fig.5.Generation of switching signals

The figure 6.shows the FPGA implementation setup for switching signals using Xilinx SPARTAN6 FPGA kit. The simulated switching signal is displayed by DSO.

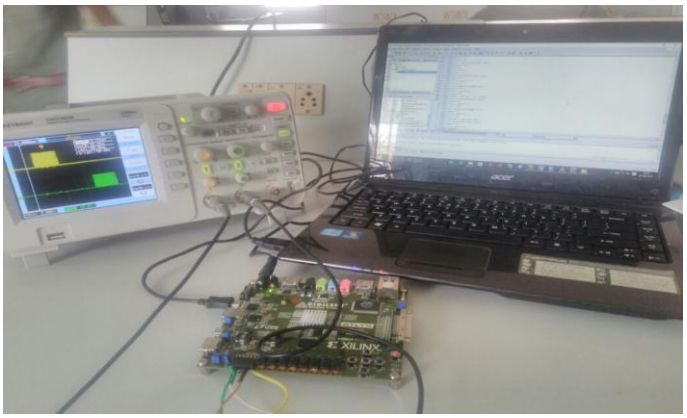


Fig.6.FPGA implement setup using Xilinx SPARTAN6 FPGA kit.

The output of generation of seven level switching signals using Xilinx Spartan 6 kit shown in the figure 7-10

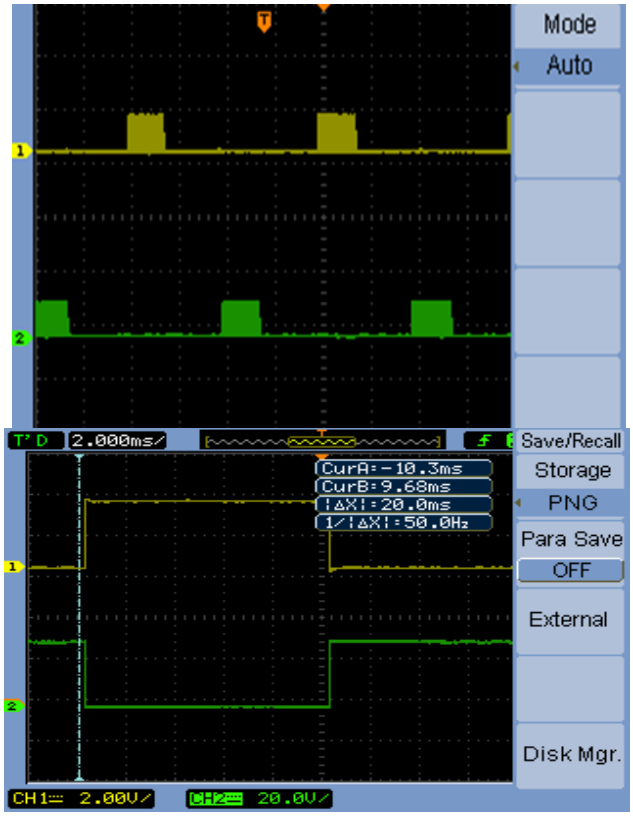
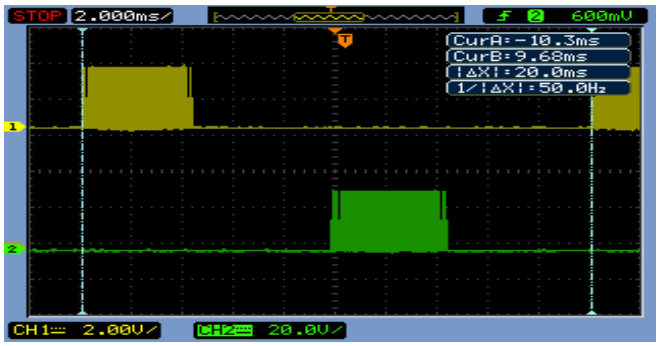


Fig 7. FPGA output of switching signals S1 and S2Fig 8.FPGA output of switching signals S3 and S4



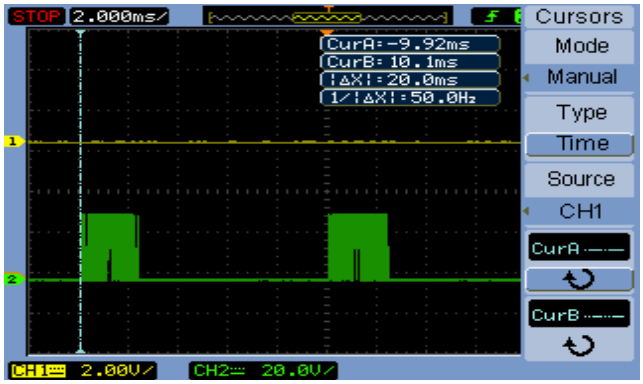


Fig 9.FPGA output of switching signals S5 and S6Fig 10.FPGA output of switching signal S7

The seven level PWM inverter which is also validated using MATLAB/SIMULINK using phase disposition switching technique. Fig 11 shows the simulation diagram of seven level PWM inverter, which includes two subsystem block. One subsystem block contains the switching pattern and other subsystem block includes the circuit diagram then RL load is connected across the output.

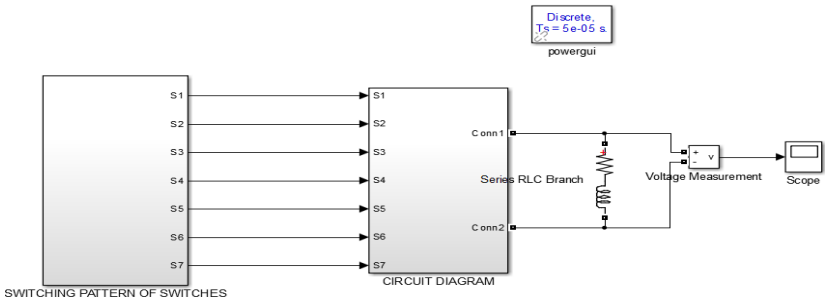


Fig 11. Simulation diagram of seven level PWM inverter

The input dc voltage is fixed to dc 150 V; hereafter, each series-linked capacitor voltage is equally energised into dc 50 V. The frequency of an output voltage is set to 60 Hz.

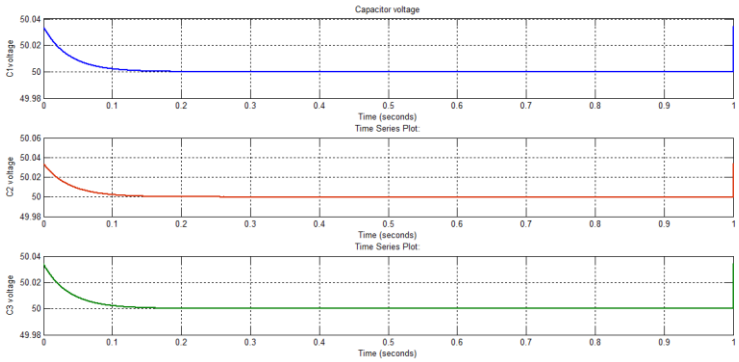


Fig 12. Output of three series-connected capacitors

By using the logical operation of command signals and switching angles according to the period seven level PWM inverter output voltage levels are generated.

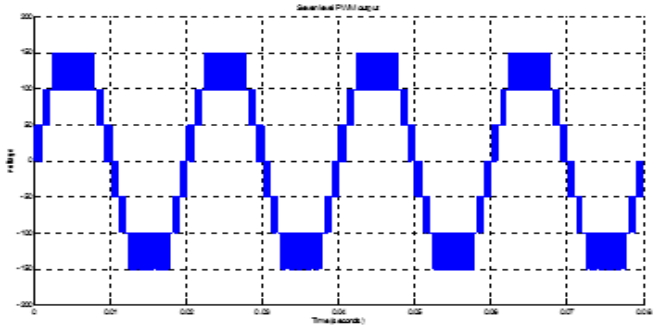


Fig 13.Output waveform of seven level PWM inverter

IV. Conclusion

In this manuscript we projected a PWM multilevel inverter that can meritoriously up surging the number of output voltage levels with a solitary dc voltage source. With the intention of produce the seven-level output voltage, the recommended multilevel inverter requires a single dc voltage source employing three series linked capacitors, two diodes, three active switches for producing the output voltage stages, and an H-bridge cell which is used to generate the polarity. The recommended 7-level PWM inverter can be a best choice, which can auxiliary for the orthodox PWM inverters.

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References

[1]. M. F. Kangarlu and E. Babaei, "A generalized cascaded multilevel Inverter using series connection of submultilevelinverters," IEEE
[2]. Trans. PowerElectron., vol. 28, no. 2, pp. 625–636, Feb. 2013.
[3]. A. Mokhberdoran and A. Ajami, "Symmetric and asymmetric design and implementation of new cascaded multilevel inverter topology," IEEETrans. Power Electron., vol. 29, no. 12, pp. 6712–6724, Dec. 2014.
[4]. S. Gautam and R. Gupta, "Switching frequency derivation for the cascaded multilevel inverter operating in current control mode using multiband hysteresis modulation," IEEE Trans. Power Electron., vol. 29, no. 3, pp. 1480–1489, Mar. 2014.
[5]. M. M. Renge and H. M. Suryawanshi, "Five-level diode clamped inverter to eliminate common mode voltage and reducedv/dtin medium voltage rating induction motor drives," IEEE Trans. Power Electron., vol. 23, no. 4, pp. 1598–1607, Jul. 2008.
[6]. J. Huang and K. A. Corzine, "Extended operation of flying capacitor multilevel inverters," IEEE Trans. Power Electron.,vol. 21, no. 1, pp. 140–147, Jan. 2006.
[7]. A. Ajami, M. R. J. Oskuee, A. Mokhberdoran, and A. Van den Bossche,"Developed cascaded multilevel inverter topology to minimize the number of circuit devices and voltage stresses of switches," IET Power Electron., vol. 7, no. 2, pp. 459–466, Feb. 2014
[8]. K.-M. Tsang and W.-L. Chan, "Single DC source three-phase multilevel inverter using reduced number of switches," IET Power Electron., vol. 7, no. 4, pp. 775–783, Apr. 2014.
[9]. J. Dixon and L. Moran, "High-level multistep inverter optimization using a minimum number of power transistors," IEEE Trans. Power Electron., vol. 21, no. 2, pp. 330–337, Mar. 2006.
[10]. K. K. Gupta and S. Jain, "Comprehensive review of a recently proposed multilevel inverter," IET Power Electron., vol. 7, no. 3, pp. 467–479,Mar. 2014.
[11]. J. Dixon et al., "Static Var compensator and active power filter with power injection capability, using 27-level inverters and photovoltaic cells," in Proc. IEEE Int. Symp. Ind. Electron., 2006, pp. 1106–1111.
[12]. M. Rotella, G. Penailillo, J. Pereda, and J. Dixon, "PWM method to eliminate power sources in a nonredundant 27-level inverter for machine drive applications," IEEE Trans. Ind. Electron., vol. 56, no. 1, pp. 194–201, Jan. 2009.
[13]. [Y. Ounejjar, K. Al-Haddad, and L. A. Greégoire, "Packed U cells multilevelconverter topology: Theoretical study and experimental validation,"IEEE Trans. Ind. Electron., vol. 58, no. 4, pp. 1294–1306, Apr. 2011.
[14]. J. Ebrahimi, E. Babaei, and G. B. Gharehpetian, "A new multilevel converter topology with reduced number of power electronic components," IEEE Trans. Ind. Electron., vol. 59, no. 2, pp. 655–667, Feb. 2012.
[15]. E. Babaei, "A cascade multilevel converter topology with reduced number of switches," IEEE Trans. Power Electron., vol. 23, no. 6, pp. 2657–2664, Nov. 2008.
[16]. K. Wang, Y. Li, Z. Zheng, and L. Xu, "Voltage balancing and fluctuation suppression methods of floating capacitors in a new modular multilevel converter," IEEE Trans. Ind. Electron., vol. 60, no. 5, pp. 1943–1954, May 2013.
[17]. E. Najafi and A. H. M. Yatim, "Design and implementation of a new multilevel inverter topology," IEEE Trans. Ind. Electron., vol. 59, no. 11, pp. 4148–4154, Nov. 2012.
[18]. Y. Hinago and H. Koizumi, "A single-phase multilevel inverter using switched series/parallel DC voltage sources," IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2643–2650, Aug. 2010.
[19]. N. A. Rahim, K. Chaniago, and J. Selvaraj, "Single-phase sevenlevel grid-connected inverter for photovoltaic system," IEEE Trans. Ind.Electron., vol. 58, no. 6, pp. 2435–2443, Jun. 2011.
[20]. A. Edpuganti and A. K. Rathore, "Optimal low-switching frequency pulsewidth modulation of medium voltage seven-level cascade-5/3H inverter,"IEEE Trans. Power Electron., vol. 30, no. 1, pp. 496–503,Jan. 2015.
[21]. J. Mei, B. Xiao, K. Shen, L. M. Tolbert, and J. Y. Zheng, "Modular multilevel inverter with new modulation method and its application to photovoltaic grid-connected generator," IEEE Trans. Power Electron., vol. 28, no. 11, pp. 5063–5073, Nov. 2013.
[22]. A. Ajami, H. Shokri, and A. Mokhberdoran, "Parallel switch-based chopper circuit for DC capacitor voltage balancing in diode-clamped multilevel inverter," IET Power Electron., vol. 7, no. 3, pp. 503–514, Mar. 20